特集

High Speed LCP Board for 28 Gbps Transmission Through 300 mm*

Circuit Board Fabrication Technology based on the PALAP Process

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Recent cloud computing communication strongly requires an order of magnitude higher bandwidth. For example, the maximum rate prescribed for SerDes and Interlaken is 28 Gbps. This trend can be observed in new enterprise servers or enterprise routers. Boards and cards for enterprise devices are often relatively large, e.g., 300 mm × 500 mm, with more than 60 layers. Fine pitch wiring of over 300 mm in length is therefore needed in each layer. We have developed an LCP board with 28 Gbps bandwidth along with a 300 mm wiring length. The board can be produced using DENSO's PALAP process, which is useful for high-density solutions involving more than 100 layers.

Key words : ultra high speed wiring, high speed PC board, I/O interface wiring

1. INTRODUCTION

On the front edge of I/O interface technology, transmission rates of 28 Gbps are starting to be used for cloud computing. New enterprise servers or enterprise routers require high performance boards or cards. These must be able to transmit at 28 Gbps over the entire length of the 300 mm wiring. In a previous paper [1] we described the development of an LCP (Liquid Crystal Polymer) board with 28 Gbps bandwidth along with a 300 mm wiring length, 100 μm width and 380 μm pitch. Here, we will additionally discuss the reason why this board showed such high performance. Several structure combinations of the board wiring will be examined in the discussion. The board can be produced using DENSO's PALAP process, which is useful for high-density solutions involving more than 100 layers.

Developing an I/O interface board with a fairly good SI (Signal Integrity) eliminates the need for complicated circuits, such as an adaptive equalizer for the transmitter and receiver, as power consumption is reduced. As reported in previous papers [2)-4)], the I/O interface circuits consume over 200 mW/lane. This is not suitable for I/O interface systems with over 64 lanes, in which a goal of low power and high bandwidth is definitely important for very large ICT centers. We have targeted and achieved a successful configuration with 32 Gbps bandwidth and sub-100 mW power needs. This paper is focused on board-level SI (Signal Integrity) matters. Another paper will be presented on low power circuit concerns with our co-design trial.

2. DESIGN CONSIDERATION BY EM SIMULATION

2.1 Material choice

A simulation was conducted to compare materials well-suited to high-speed signaling. The three materials considered are shown in **Table 1**.

Table 1　Consideration of dielectrics for the board

Material	Dielectric constant	Dielectric loss factor	Test frequency
BCB*	2.23	0.0005	77 GHz
LCP**	2.9	0.0022	25 GHz
FR-4	4.2	0.015	3 GHz

*BCB:Benzo-cyclo-butene, **LCP:Liquid Crystal Polymer

As shown in **Fig. 1**, simulated wiring patterns were taken as actual routing from surface pad to inner-layer wiring and then back to the surface pad, with a 300 mm length, 100 μm width,

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60 μm spacing, and 18 μm thickness.

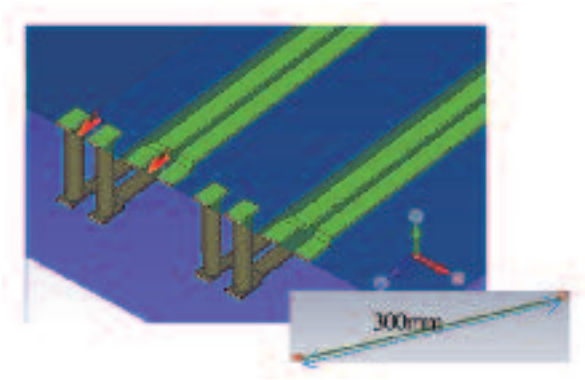


Fig. 1　Simulation pattern for 300 mm wirings

The eye pattern simulation results for the three materials in the case of a mirror interface between copper and dielectric is shown in **Fig. 2**. Although we found that the best profile was achieved with BCB, this was for boards that did not require around 100 stacked layers. As we have established a relatively good LCP board and a production process named PALAP, we chose the LCP dielectric material for the examination board on this occasion.

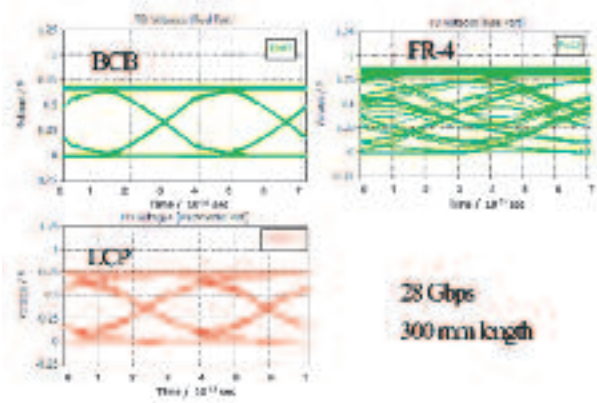


Fig. 2　Eye pattern profile of 28 Gbps by EM-simulation

2.2　Copper interface effect

For signal transmissions exceeding 10 Gbps, the skin effect poses a serious problem as it degrades SI. We also conducted an EM simulation with 3 μm roughness added to the above-mentioned mirror surface interface between copper and FR-4 or LCP dielectric, as per the structure in **Fig. 1**. **Fig. 3** presents our simulation results and the marked difference between the two.

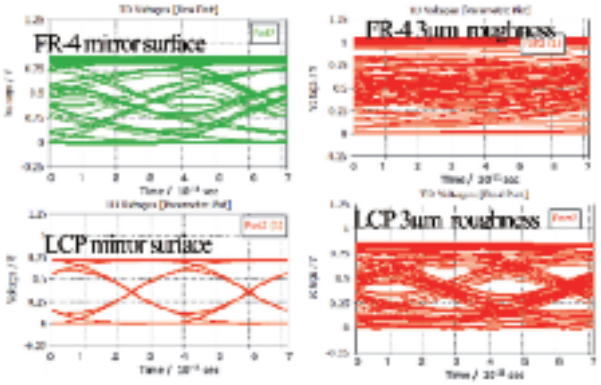


Fig. 3　Transmit signal after 300 mm length at 28 Gbps.

2.3　Effect of shielding by GND plane

The actual boards of enterprise servers or enterprise routers need various kinds of wirings, such as control lines. In many designs, a GND plane or power plane is used for the shield layer between high-speed lines and others. So, we have to evaluate the effect of shielding high-speed lines by upper layer and lower layer planes as shown in **Fig. 4**.

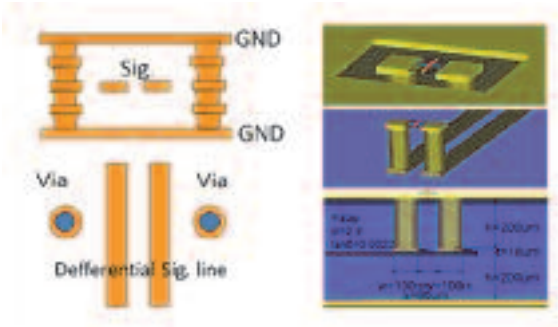


Fig. 4　Shielded differential signal line

3.　TEST METHOD FOR 28 GBPS

3.1　Feature of test coupon

To achieve a high baud rate of digital signals similar to an actual wiring route on a PC board, the test coupon of the LCP board was designed as a 10-layer structure on a 150 mm × 150 mm square, as shown in **Fig. 5**. The 300 mm length of the longest wiring is routed with four turns at the surface and within one of the inner layers. The two paired wirings with differential transmission lines (Z0=100 ohm) were designed with a 100 μm line width and 60 μm spacing. To examine the cross-talk effect, an adjacent differential transmission line was installed with 120 μm spacing in parallel with it. These dimensions could enable fairly fine pitch design (380 μm) and are excellent for a complex, high-den-

sity system. The thickness of each LCP layer was 100 μm, with 100 μm × 150 μm overwrapped twin vias for layer interconnection. The width of the via land was only 100 μm, equal to the line width and optimal for minimizing the impact of high band transmission circuits. Wiring thickness was as thin as 18 μm, which imposes a relatively small stress on metal wiring. LCP is an excellent material for high speed signaling, and has a dielectric constant of 2.9 and dielectric loss factor of 0.0022 at 25 GHz.

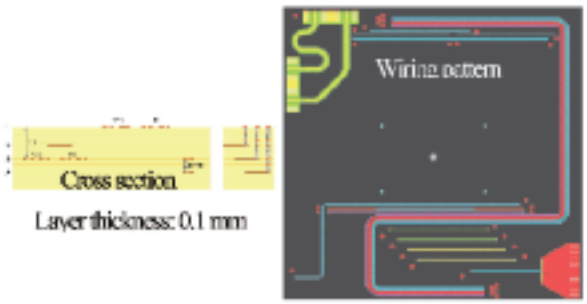


Fig. 5　Test coupon made by LCP and mirror surface Cu

The high-performance LCP (Liquid Crystal Polymer) Board is available for production. The basic PALAP process allows for 100-layer configurations and embedded Chip-Capacitors, as shown in **Fig. 6**. As the substrate material, it uses the one-sided copper clad film of the thermoplastic polymer LCP. This thermoplastic copper clad film has excellent dimensional stability and very long storage life. After forming a pattern by conventional photo-etching, vias are formed on the copper land with a laser drill. The vias of each sheet are filled with a metal paste composed of Sn/Ag powder and organic solvent. The aligned sheets are pressed simultaneously with a hot vacuum press. The heat and pressure of the hot press not only bond each via but also create adherence between each thermoplastic sheet.

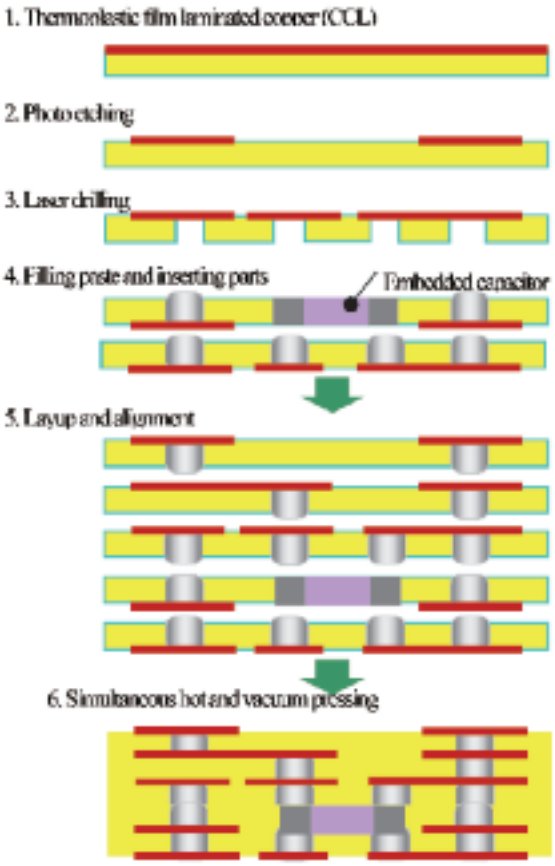


Fig. 6　Basic PALAP process

We modified the basic PALAP process to a high speed specification as follows :

(1) Wiring routing design was maintained to exactly 100 ohm of characteristic impedance, even in via holes. An overlapped twin via structure was its key element.

(2) The interface between copper wiring and LCP dielectric should be as smooth as possible, with strong adhesion. A sub 1 μm roughness was maintained.

(3) The wiring edge shape on the etching process should be relatively straight for the whole length. The 90-degree turn was to achieve a smooth, rounded design.

3.2　Method of measuring setup

Measurement of signals exceeding 10 Gbps requires careful selection of the apparatuses, connection wiring, connectors and probes, preferably with specifications over 40 GHz. Our setup as shown in **Fig. 7** and **Fig. 8** targeted SI measurement of 28 Gbps, which was sufficient for our purposes. The method involved extracting data from the S-parameter

obtained from the 6 ps rise time step signal generation for measuring from DC to 40 GHz.

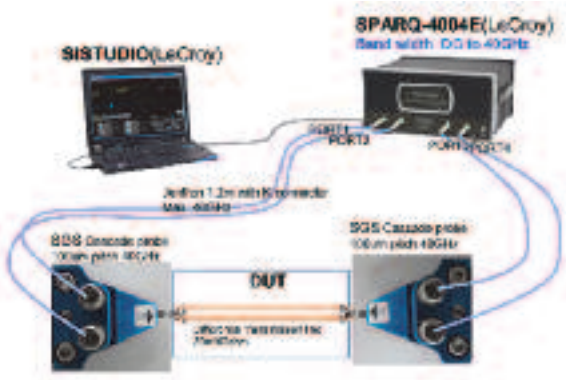


Fig. 7　Apparatus and connection for high specification

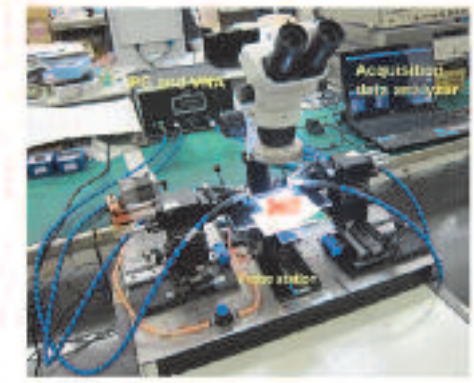


Fig. 8　Measurement setup

4.　RESULTS AND DISCUSSION

4.1　Results for signal integrity

The measurement resulted in 30 Gbps bandwidth at random pulse input (PRBS 10^7) on 300 mm of inner layer wiring with a 0.9 μm roughness wiring surface, as shown in **Fig. 9**. The open eye can be seen even at 30 Gbps, which indicates a level at which our configured receiver would receive as a proper signal.

Fig. 10 shows the comparison between 0.9 μm and 0.45 μm surface roughness on surface wiring. The effect of wiring roughness is clearly shown to be similar to the simulation tendency (**Fig. 3**).

Fig. 11 shows measuring eye-pattern and transmission loss characteristics of a shielded differential signal line and an unshielded line. The loss seen in the shielded differential line is not so large as compared to the unshielded line. In standard designed boards, it seems to be increase the loss due to coupling between the GND plane and signal lines. However, the smooth surface copper foil and the low-loss material were confirmed to be advantageous for suppressing the increase of these loss-factors.

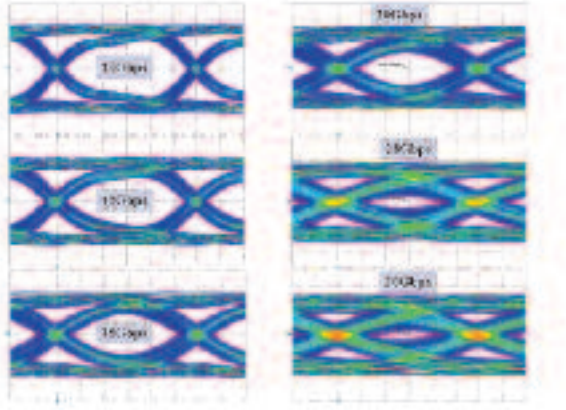


Fig. 9　Measuring eye-pattern on 300 mm length inner wiring with 0.9μm surface roughness at several rates

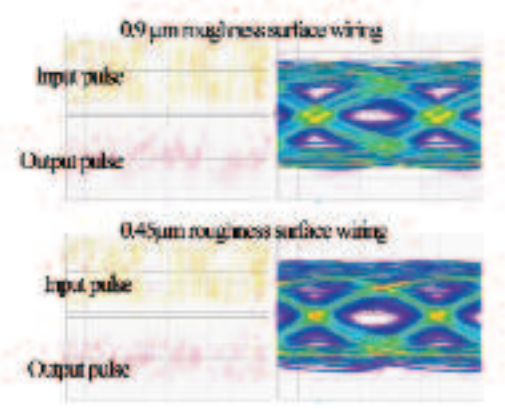


Fig. 10　Measuring eye-pattern on 300 mm length wiring with 0.9μm and 0.45μm surface roughness at 30 Gbps

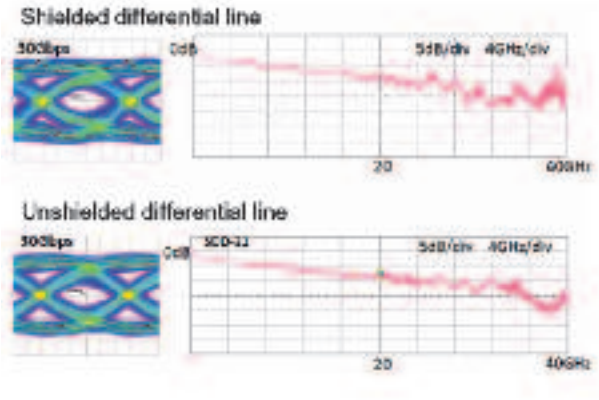
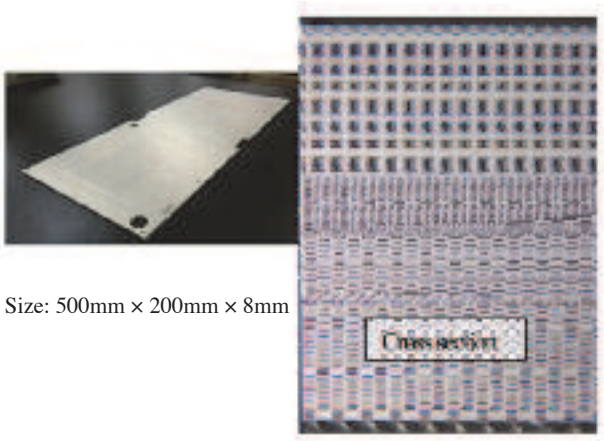


Fig. 11　Measuring eye-pattern and loss characteristics on 300 mm length, 100μm width shielded differential line

4.2　Board structural capability

A conventional PALAP board, a general LCP board with 129 layers for specific use, is shown in **Fig. 12**. This process technology has already been established in production, and it has even been possible to embed parts without warpage. Modifying the technology to a higher speed specification as mentioned in section III-A above could make faster products possible.



Size: 500mm × 200mm × 8mm

Fig. 12　PALAP processing board with 129 layers

5.　CONCLUSION FOR 28 GBPS BANDWIDTH

As a key technology, higher performance was achieved by using LCP material, making same size vias with the same wire width, achieving a smooth wiring surface, and routing the inside and surface layers.

In a wide range of wiring lengths to a maximum of 300 mm, we confirmed that a high performance of 30 Gbps can be expected to be achieved even if the signal lines are shielded by GND plane layers, and thus fulfill the actual design needs of computer hardware. This approach definitely suits 28 Gbps cloud system applications.

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