A double gate normally-off silicon carbide (SiC) trench junction field effect transistors (JFET) design is considered. Innovative migration enhanced embedded epitaxial (ME3) growth process was developed to replace the implantation process and realize high device performance. Strong anisotropic behavior in electrical characteristics of the pn junction fabricated on (11-20) and (1-100) trench a-planes was observed, although quality of the pn diodes was found to be independent of trench plane orientations. Fabricated normally-off trench 4H-SiC JFET demonstrates the potential for lower specific on-resistance (Ron) in the range of 5-10mΩcm² (1200V class). A relative high T-dependence of Ron is observed. A breakdown voltage of about 400V in the avalanche mode was confirmed at zero gate bias conditions for cell design without edge termination. It was demonstrated that the normally-off JFETs are suitable for high temperature applications. Average temperature coefficient of threshold voltage (Vth) was calculated as -1.8mV/°C, which is close to the MOS based switching power devices.

**Key words**: Silicon carbide, Embedded epitaxy, JFET, Normally-off, High temperature operation

1. **INTRODUCTION**

Wide band gap SiC-JFETs are attractive switching device option for high temperature power applications as they are free from gate oxide, however, SiC-MOSFETs working at more than 200°C temperature will definitely raise severe questions about Vth stability and MOS gate reliability. SiC-BJTs need high input power, increasing with temperature and comparably poor switching speed of BJTs is an additional limiting factor. Normally-on (depletion-mode) JFETs have already demonstrated their unequalled low Ron while being capable of operating at cryogenic and high temperature at high switching speed. However, these switching devices require sophisticated gate control circuits. On the other hand, normally-off (enhancement-mode) JFETs face issues related to the gate control due to limited available gate voltage range, compare to conventional MOS based switching power devices and therefore suffers from low immunity to electro-magnetic interference (EMI) noise. In general, these switching devices, independent of their mode of operations require special gate control circuits for reliable operations. For high temperature automotive and aerospace applications in the temperature range above 200°C (Tj= 300°C), ultra-low-loss SiC switches i.e., Ron below 5mΩcm² with high stable Vth will have a chance to replace the existing Si insulated gate bipolar transistor (IGBT) technology.

In this paper, we discuss a double gate normally-off SiC-JFET key technologies starting from the device design to innovative fabrication process. All-epitaxial grown normally-off trench SiC JFET design is considered. Ion-implantation technique has been used as the only viable means for selective area doping so far. However, the ion-implantation induced structural damage and anisotropic diffusion during the annealing are inevitable problems that yield poor pn junction performance viz., lower built-in-potentials and higher pn junction reverse leakage current. SiC epitaxial growth has been a key device process technology and contributed greatly in the development of power devices despite relatively poor quality of the 4H-SiC substrates. Several attempts have been done in the past to develop the selective embedded epitaxy process for device application. We have developed a non-masked selective epitaxial growth process called migration enhanced embedded epitaxy (ME3) process to realize selective doping for device application. This innovative process is the key to realize the high performance normally-off trench 4H-SiC JFETs.

2. **NORMALLY-OFF JFET DESIGN**

A schematic cross-section view of double gate normally-off
off trench SiC-JFET is shown in Fig. 1. Compared to the conventional JFET structure, the new design feature consists of an embedded top trench gate structure. The n-type channel and p-type gate layer were grown epitaxially in the trenches to fabricate all epitaxial JFET structure. Top trench gate doping level and depth can be controlled independent of the buried gate specification in this JFET structure.

Fig. 1 A schematic cross-section view of double gate normally-off trench SiC-JFET

This feature allows the freedom for (i) Design of cell blocking voltage, and (ii) Option of integrating pn/Schottky diode in a selected area as integrated diode or to make it more robust at high temperature operations.9 Designed normally-off JFET support the desired blocking voltage by relying on the potential barriers established by the buried and top gate junction, thus avoiding a complex gate circuitry. Design details are given elsewhere.9 Top trench gate pn junction was designed considering the trench a-plane crystallographic orientations and high built-in-potential requirements of normally-off JFET. An innovative ME3 is developed to grow realize highly doped epitaxial top trench gate structure.

3. KEY FABRICATION TECHNOLOGY: ME3 GROWTH PROCESS

Innovative ME3 process consists of 2-phases viz., (i) Pre-deposition etching process, and (ii) Deposition process, which basically consists of the heating up phase, etching phase, growth process phase, and cool down phase. The pre-deposition etching process involves the preparation of non-planar surface with H2 or HCl etching, depending on the CVD reactor i.e., Cold-wall or Hot-wall configuration. The main technology around the developed key process utilized the epitaxial process under (i) High growth temperatures \( \geq 1600^\circ C \), (ii) Low C/Si ratio, (iii) Low growth rates, and (iv) High pressure to control the anisotropic growth dependence. Figure 2 shows the cross-sectional SEM images of n-type trenched substrate aligned along the \([11-20]\) direction filled with n-type epitaxial layer.

Fig. 2 Cross-sectional SEM images of trenched substrate filled with n-type epitaxial layer grown using ME3 growth process at various growth intervals: (a) starting n-type trenched substrate (With bottom Al-implanted marker), (b) after 20 min., (c) 40 min., and (d) 90 min.
grown at temperature \( \geq 1600^\circ \text{C} \) at various time intervals.\(^7\)

It is evident from the images that epitaxial growth at the bottom of trenches is greatly enhanced compared to growth on the sidewalls under the said growth conditions. The growth inside the trenches is nearly 3-times higher than that mesa area, which is attributed to the large surface diffusion length of reactant species mainly due to the higher growth temperature. Similar growth behavior was observed for stripe-trench structures aligned either along the \([11-20]\) or \([1-100]\) directions. It seems that the \( ME^* \) growth process does not follow the basic orthodox step-flow mechanism. The \( ME^* \) process will be an alternative processing solution of high temperature ion-implantation process, which still suffers from the implantation induced defects. Also, this innovative process will be a key process technology for future SiC reduced surface field (RESURF) power devices.

4. EPITAXIAL PN FABRICATION AND ELECTRICAL CHARACTERISTICS

To investigate the trench a-plane crystallographic orientations dependence on the electrical performance of top trench gate, pn diodes were fabricated on \((1-20)\) and \((1-100)\) trench a-planes. Trenches with a hexagonal pattern (Typical pn junction active area is about \( 6 \times 10^4 \text{ cm}^2 \)) were formed on 4H-SiC \((0001)\) Si face substrate by RIE. The stripe trenches were aligned along the \(<11-20>\) or \(<1-100>\) direction. The pn diodes were fabricated by embedded epitaxial growth of 0.1 - 0.5 \( \mu \text{m} \) thick undoped layer, which is followed by the growth of 1.0 \( \mu \text{m} \) thick highly Al-doped (Na: 1.0 - 5.0 \( \times 10^{19} \text{ cm}^{-3} \)) p-type layer. Ni and Ni/Al contacts were deposited as the n-type and p-type Ohmic contact metal, respectively. All contacts were sintered at about \( 1000^\circ \text{C} \) for 5min. using RTA (Rapid Thermal Annealing), and thick Ti/Au layers were used for pad metals. Forward and reverse current-voltage (I-V) measurements were carried out on fabricated 4H-SiC pn junction diodes as shown in Fig. 3. Forward I-V of pn junction diodes formed on either oriented stripe geometry shows good electrical characteristics with an ideality factor of nearly 2.0 and are comparable to classical planar diodes. No excess leakage was observed for pn junction diode on \([1-100]\) trench sidewalls, which is usually attributed to the poor quality of the epitaxial layers. Reverse current density at voltage around - 40 to -50V is less than \( 10^4 \text{A/cm}^2 \), indicating excellent pn junction diode properties. The pn junction diodes on \([11-20]\) trench sidewalls show higher breakdown voltage, which is attributed to the less incorporation of N-donors on \([11-20]\) trench sidewalls and \( (0001) \) plane compared to the \([1-100]\) trench sidewalls and \((0001)\) plane. Such an anisotropic behavior in the breakdown voltage of pn junction diodes fabricated by embedded growth due to the crystallographic orientation of trenches is observed for the first time to our knowledge.

![Fig. 3a Forward I-V characteristics of pn diodes fabricated on trenched a-planes](image1)

![Fig. 3b Reverse I-V characteristics of pn diodes fabricated on trenched a-planes](image2)

5. JFET FABRICATION AND ELECTRICAL CHARACTERISTICS

Double gate normally-off trench SiC-JFET devices were fabricated on n-type \((0001)\) oriented Si-face 8 degree-off 4H-SiC substrates. Four epilayers were grown on n-type substrates in a single growth run. The drift layer was about 13 \( \mu \text{m} \) thick, N-doped \((\text{Nd: } 3.0 - 5.0 \times 10^{19} \text{ cm}^{-3})\) n-type layer. The buried gate layer was grown on the top of the drift layer. The buried gate layer was 1.5 - 2.0 \( \mu \text{m} \) thick, Al-
doped (Na: 0.1 - 1.0×10^{19} \text{cm}^{-3}) p-type layer. The buffer layer was 0.1 - 0.5 \mu m thick, non-doped layer followed by the finally about 1.0 \mu m thick, N-doped (Nd: 1.0 - 2.0×10^{19} \text{cm}^{-3}) n-type source layer. JFET trench gates were nearly perpendicular (about 87 deg.) to the primary flat of the SiC wafers. Trenches of about 4 \mu m were formed by inductive coupled plasma (ICP) dry etching process. The n-type and p-type epitaxial layers were sequentially embedded in the trenches to define the typical 0.2 - 0.5 \mu m thick, N-doped (Nd: 0.1 - 1.0×10^{17} \text{cm}^{-3}) n-type channel epi-layer and the embedded Al-doped (Na: 0.1 - 1.0×10^{19} \text{cm}^{-3}) top gate layer, respectively. The channel region is sandwiched between the Al-doped planar buried and embedded top gate layers. The drain to source conduction is regulated by the channel depletion width, which is controlled by the buried and top gate bias conditions. This process sequence is followed by necessary selective etching or planarization process before the metal contact formation. Ni and Ni/Al contacts were deposited as the n-type and p-type Ohmic contact metal, respectively. All contacts were sintered at about 1000\,^\circ \text{C} for 5\min. using rapid thermal annealing (RTA) furnace, and thick Ti/Au layers were used for pad metals. The typical active area of the 12 \mu m stripe cell design JFET is about 1.58\times10^{-4} \text{ cm}^{2}. In the present investigations, normally-off JFET devices are fabricated without the cell edge termination structure.

**Figure 4** shows the forward drain current-drain voltage (ID-VD) characteristics of a typical normally-off trench 4H-SiC JFET at room temperature. The device was fabricated without edge termination structure using a n-type drift layer about 13 \mu m thick with the blocking capabilities of more than 1200\,V. A breakdown voltage of about 400\,V in the avalanche mode was confirmed at gate bias condition of VG=0\,V. This breakdown voltage is consistent with the simulated values for a trench JFET cell without edge termination structure. Typical Ron at drain voltage VD=2.0\,V and gate bias voltage VG=2.5\,V has been measured in the range 5 - 10\,m\Omega \text{cm}^{2} at the wafer level. This variation in the Ron was attributed to the process variation on the wafer scale fabrication. The typical Vth was below 1.0\,V at the wafer level (around 0.5\,V - 0.6\,V).

**Figure 5** shows the temperature dependence of ID-VD (at applied VG=2.5\,V) and Vth (at applied VD=0.5\,V) characteristics in the range from room temperature (25\,\degree \text{C}) to 250\,\degree \text{C}. At room temperature, almost all the N-donors are ionized and Ron is defined by the electron mobility, therefore, an increase in temperature results in a decrease in ID, thus an increase of the Ron as shown in **Fig. 5**. The Ron increased by a factor of 3 - 4 in the measured temperature range of 25 to 250\,\degree \text{C}, resulting in negative temperature coefficient. The T^{-2.6} dependence of Ron is observed for the fabricated normally-off trench 4H-SiC JFET. This high value of \alpha=2.6 is close to the Si power devices of similar class, however, higher compare to the values reported for SiC devices. These results indicate a strong domination of phonon scattering in device carrier mobility. The temperature dependence of the fabricated normally-off 4H-SiC JFET Vth is also shown in **Fig.5.** The Vth (at applied VD=0.5\,V) monotonically decreases with increasing temperature from room temperature. In some cases, the Vth changes from positive to negative and the JFET turns from a normally-off device into a normally-on device. At this stage, the JFET is not

![Fig. 4 ID-VD characteristics of a typical normally-off trench 4H-SiC JFET at room temperature (cell without edge termination structure)
fully pinched off at zero gate bias but has the Ron high enough to protect the device and circuit by limiting the forward ID low enough in the event of abnormal operating conditions i.e., gate control failure. The typical Vth at room temperature is about 0.6V and decreases to about 0.2V at 250°C. Average temperature coefficient of Vth was calculated as -1.8mV/°C, which is close to the ideal values for MOS based power switching device due to absence of any kind of interface states. The difference in the Vth in the entire measure temperature range is only about 0.4V and most of the devices are still normally-off. In low temperature region, it is expected that Vth will increase with decreasing temperature due to reduction of ionization ratio of the N-donor and subsequently devices will maintain the normally-off operations. In other words, normally-off JFETs are more robust in low temperature region.

6. SUMMARY

In this paper, we have proposed a double gate normally-off trench 4H-SiC JFET design. An innovative ME$^2$ growth process was developed to replace the implantation process and realize high device performance. The crystallographic orientation of the trenches has been found to be important for device design consideration, although similar performance was achieved for (1-100) and (11-20) a-planes. Electrical characteristics of fabricated trench 4H-SiC JFETs at high temperature were discussed and it is demonstrated that normally-off JFETs can operate up to 250°C. A breakdown voltage of about 400V in the avalanche mode was confirmed at zero gate bias conditions for cell design without edge termination. Typical Ron at room temperature was 5 - 10m$\Omega$cm$^2$ at VD=2.0V (VG=2.5V) for the 12µm cell design. A relative high T$^{-2.6}$ dependence of Ron is observed for the fabricated 4H-SiC JFET. Nearly ideal temperature dependence of Vth is realized using the all-epitaxial structure and was attributed to higher pn junction built-in-potential and lower reverse leakage current. These results demonstrate that the normally-off JFETs are suitable for high temperature applications.

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