This study seeks to analyze the reliability of three-dimensional (3D) chip stacked packages under cyclic thermal loading. The critical areas of 3D chip stacked packages are defined using Finite Element Modeling (FEM) based simulations to correlate the thermal cycling experiments.

3D chip stacked packages consist of two 300µm thick Si chips vertically connected with Sn-Ag-Cu solder bump joints and then assembled on a conventional FR-4 printed circuit board (PCB). Two thermal cycle conditions were studied, namely -40 to 125°C and 0 to 100°C. FEM simulations indicate that in both conditions, the critical failure location is expected to be the chip side region of the corner solder bump of the lower chip connecting the package to the PCB. Creep strain per single thermal cycle averaged over a critical damage volume; \( \Delta \varepsilon_{cr} \) was used as the damage parameter.

Furthermore, we have investigated possible approaches to improve the thermo-mechanical reliability of this package. The results indicate that adding an underfill or thinning the Si chips will achieve a lower creep strain in the solder bumps. Furthermore, the stress levels in the Si and Cu via in the Si chip are low. Therefore fracturing of the Si chips and fatigue of the Cu vias is not expected under thermal cycling conditions.

**Key words**: Thermal cycle, 3D chip stacked package, Pb-free solder, Parameter study, FEM analysis

1. **INTRODUCTION**

In a three-dimensional (3D) package, semiconductor devices or packages are stacked in the vertical direction. This package is effective in the reduction of a mounting area. Several 3D packaging concepts have presented in the literature and some types of 3D packages are already in fabrication.

3D chip stacked packages with bumps can more effectively minimize the mounting area on a PCB. Furthermore, by connecting the chips with through vias, the resulting reduction in the wiring length allows a faster transmission of the electric signal. Normally, the chips in this package are thin and have many I/Os. This leads to some issues, such as the handling of thin Si wafers during production, bending of devices and a need for improvement of alignment accuracy between devices.

In this study, we have investigated the reliability of the 3D chip stacked package with two Si chips of 300µm thickness and Sn-Ag-Cu solder bump joints (300µm diameter). Furthermore, we have investigated the possibility of increasing the reliability of this package using finite element model FEM (Finite Element Model) simulation.

2. **SAMPLE PREPARATIONS**

The demonstration device consists of two Si chips connected vertically with Sn-Ag-Cu solder balls. The bottom Si chip has a daisy chain on the lower face in order to allow in-situ four-point measurement of resistance during accelerated temperature cycling test. The chips have 8×8 area array of solder pads with a 1mm pad pitch.

The Si chips are assembled on a FR-4 PCB (printed circuit board) with Sn-Ag-Cu solder balls (Fig. 1). The dimensions of the Si chip are 10×10×0.3mm³ and the diameter of the solder ball is 300µm.

The daisy chain on the bottom chip is formed with plated-Cu circuit and BCB (Benzocyclobutene) is used as a solder mask to restrict the solder pad openings. The thicknesses of both Cu and BCB are 5µm with copper pads of 500µm diameter and 250µm BCB opening. On the other side of chip, a blanket layer of electroplated copper is deposited and BCB openings which mirror the lower side are formed.

The thickness of PCB is 2.5mm. The thicknesses Cu and solder mask on PCB are 50µm, and the diameters of them are 250µm and 300µm, respectively.
The reflow profile has a peak temperature of 240°C and the time above liquidus is 60 seconds in an air atmosphere.

After assembly, the quality of the connections is confirmed with X-ray inspection, cross sectioning and the electric resistance measurement of the daisy chain.

3. FEM MODELING

FEM simulations are performed in order to predict a failure mode and as a second stage, to optimize the structure. Figure 2 shows 3D FE model and close up of the critical bump. Due to the symmetry, only one-eighth of the structure needs to be modeled. All processing; modeling, solving and post-processing tasks are performed using the commercial FE code MSC.MARC.

The material properties used in the model are listed in Table 1. Except for Sn-Ag-Cu solder and Cu, all the materials are modeled with isotropic, linear, elastic properties. The equation for the creep strain of Sn-Ag-Cu material is shown below:

\[
de = \frac{2 \times 10^5 \sigma e}{\exp \left( -\frac{9994.59}{T} \right)}
\]

where \( e \) is creep strain, \( t \) is time in second, \( \sigma \) is stress in MPa and \( T \) is temperature in K. The temperature dependent Young’s modulus of Sn-Ag-Cu and the yield stress of Cu are also listed in Table 1.

The materials of the structure are assumed to be stress-free at 25°C. Cyclic thermal loads with temperature excursions of -40 to 125°C and 0 to 100°C, at the frequency of 1 cycle per hour are applied.

Furthermore, it is assumed that, the shape of Si chips is perfectly flat before the thermal cycle, although in reality, the Si chips may have some inherent bending induced by the stress from a grinding and thin film deposition.

4. RESULTS AND DISCUSSION

4.1 3D 300μm-thickness-Si-chip stacked package

Figure 3 shows the view of Si chip with a daisy chain and Sn-Ag-Cu solder balls. The two Si chips are connected vertically as shown in Fig. 4. Optical and SEM image analysis indicates a sufficient formation of intermetallic layers to enable a good solder joint formation on both the package and the board side.

In Fig. 5, the deformation and the von Mises stress of the 3D chip stacked package during a thermal cycle test (-40 to 125°C) is shown. Due of the mismatch of coefficient of thermal expansion (CTE) between Si and PCB, the solder bumps, especially between 1st Si and PCB (1st bumps) are deformed. On the other hand, the solder joints between 1st Si chip and 2nd chip (2nd bumps) have hardly deformed, because the relative displacement between the 1st and 2nd Si chip is at the same level during the thermal cycle and these
solder joints see very little strain imposition.

**Figure 6** shows the accumulated creep strain in the critical corner bump on PCB after 3 cycles of -40 to 125°C. It is observed that the maximum creep strain is located in the upper part of the solder joint, close to 1st silicon chip. As a damage parameter, we chose $\Delta \varepsilon_{cr}$ (creep strain averaged over a damage volume per one thermal cycle) in 3rd cycle. For the calculation of $\Delta \varepsilon_{cr}$, a damage volume of three (upper part) or two layers (bottom part) of elements, as shown in **Fig. 6**, are selected.

In Table 2, the results of $\Delta \varepsilon_{cr}$ are shown. In both thermal cycle conditions, $\Delta \varepsilon_{cr}$ of the 1st bump (on PCB) is higher than the 2nd bump (between Si chips) and the upper part shows a greater strain accumulation than the lower part. Thus failures resulting from thermal fatigue fracture are most likely to occur in this region of the upper of the 1st solder bump during thermal cycle.

Moreover, in **Fig 7**, the stress in Si chips in the package at 125°C is shown. The maximum stress is 106MPa and mainly concentrated on the 1st silicon chip and in the area close to bumps. Since this stress level is much less than the critical fracture stress, the fracture of Si chip is not expected during thermal cycle. However it must be noted that this analysis assumes perfect defect-free silicon and that processing related defects such as excessive chip chipping during saw singulation or excessive roughness during backgrinding may create local stress concentration points which could initiate fracture.

Thus from FEM simulations, we expect that the 3D chip stacked package is most likely to fail from solder joint fatigue in the upper part of 1st solder bump at the corner of the chip during thermal cycle.

We will analyze the reliability and failure mode of the real demonstrator and compare these FEM results.
In a real 3D chip stacked package, Cu via holes are formed in Si chips to connect Si chips electrically. In this case, the thinner Si wafer is preferred, because it is easier to form via holes.

The behavior of the 3D chip stacked package with Si chips of different thickness by FEM simulation is analysed in this section. In this analysis, we choose thermal cycle condition -40 to 125°C and use the same FE model with varying chip thickness. 'JHVSF shows ∆ε in the critical 1st bump on PCB when the thickness of Si chip is changed from 50µm to 400µm. The thinner Si chips result in a lower ∆ε in solder bumps. This is attributed to the fact that the thinner chips have less stiffness and the imposed deformation on the solder joint is thus lower.

However, the maximum creep strain in the package is still high (5.12%), so we will need to find the solution to decrease the strain in the solder joint.

On the other hand, the von Mises stress in the Si chip increases when the chip becomes thinner (Fig. 9). Nevertheless, the maximum stress reached is 188MPa. Therefore, the fracture of Si chips is not expected during the thermal cycle test even if thinner Si chips are used.

4.3 Stress of Cu via hole in Si chip

During manufacturing and subsequent thermal loads, Cu via holes are subjected to thermal stresses and strains. If a higher strain or stress is generated in the via hole, it would be a driving force for fatigue crack initiation and
propagation to failure.

For this purpose, a FE model with Cu via holes and Cu re-distribution paths was constructed. Figure 10 shows a partial view of this model for this. The thickness of Si chip is 100µm and the diameter of via hole is 50µm. And the diameter of Sn-Ag-Cu solder ball for 2nd bump is 130µm. Other dimensions are the same as Fig. 2.

Figure 11 shows the von Mises stress in the Cu via hole, re-distribution paths and pad around 1st Si chip at 125°C. The stress in Cu is the largest at 125°C during thermal cycle. From this result, the stress of Cu in via hole is less than 145MPa and problems with Cu are not expected.

We will compare this FEM simulation result with measurements of real sample in the future work.

4.4 Effect of underfill

From the results mentioned above, thin Si chip is expected to decrease the creep strain in solder bumps and improve the life-time of the 3D chip stacked package. However, the $\Delta\epsilon_c$ value is still high. An option to reduce the high strain levels is to use an underfill.

Figure 12 shows the FE model with under-fill. An underfill layer is applied in the gap between the 1st Si chip and the PCB. Table 3 shows material properties of two types of underfill used in the simulation. In this model, the contact analysis, feature implemented in MSC.MARC software is applied. Contact (glue) mode is applied boundaries between underfill and solder mask and underfill and Si chip. The other dimensions are the same as Fig. 10.

Figure 13 shows $\Delta\epsilon_c$ in 1st bump and 2nd bump at corner,
with Sn-Ag-Cu solder bumps. The FEM simulation result shows that the failure position is expected the top part of the critical solder bump joining the lower chip and the PCB during a thermal cycle test.

Furthermore, the possibility of improvement of the thermo-mechanical reliability for the package is investigated. The study shows that thinner Si chip and use of under-fill can decrease the $\Delta \varepsilon_{cr}$ in solder bumps.

**ACKNOWLEDGEMENT**

The authors would like to thank IMEC and DENSO CORPORATION for support and permission to publish this work. The authors also would like to thank Tomas Webers, Philippe Soussan, Piet de Moor, Koen de Munck and Jurgen Hendrickx for the technical support for designing and fabrication of the stacked devices.

**REFERENCES**

＜著者＞

則武 千景
（のりたけ ちかげ）
生産技術開発部
エレクトロニクスの実装技術開発
に従事

Paresh Limaye
Paresh Limaye is currently pursuing his PhD in Mechanical engineering at the Catholic university of Leuven, Belgium with the support of IMEC. The focus of his PhD involves material characterization, reliability and finite element analysis for lead free soldering applications.

Mario Gonzalez
Mario Gonzalez received his PhD degree in Mechanical and Materials Engineering from the Ecole Centrale Paris in France. Since then, he joined IMEC, in Belgium as Research Engineer. His research interests include thermomechanical reliability aspects, advanced packaging technologies and numerical Finite Element Simulation.

Bart Vandevelde
Bart Vandevelde received a PhD degree from the Catholic University of Leuven (Belgium). Currently, he is responsible at IMEC for the thermal and thermo-mechanical modelling team and is coordinating several bilateral, European and Flemish projects for IMEC.